Refine Search

Search Results -

Terms	Documents
L3 and (switch same memory same interfac$3)	99

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L5

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Monday, May 09, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
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L5	L3 and (switch same memory same interfac$3)	99	L5
L4	L3 and switch	357	L4
L3	L2 same cache	679	L3
L2	L1 same memory	3899	L2
L1	((disk or disc) near05 controller) same (host or computer or CPU) same interfac$3	6955	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
L5	0

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L6

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Monday, May 09, 2005 Printable Copy Create Case

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DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
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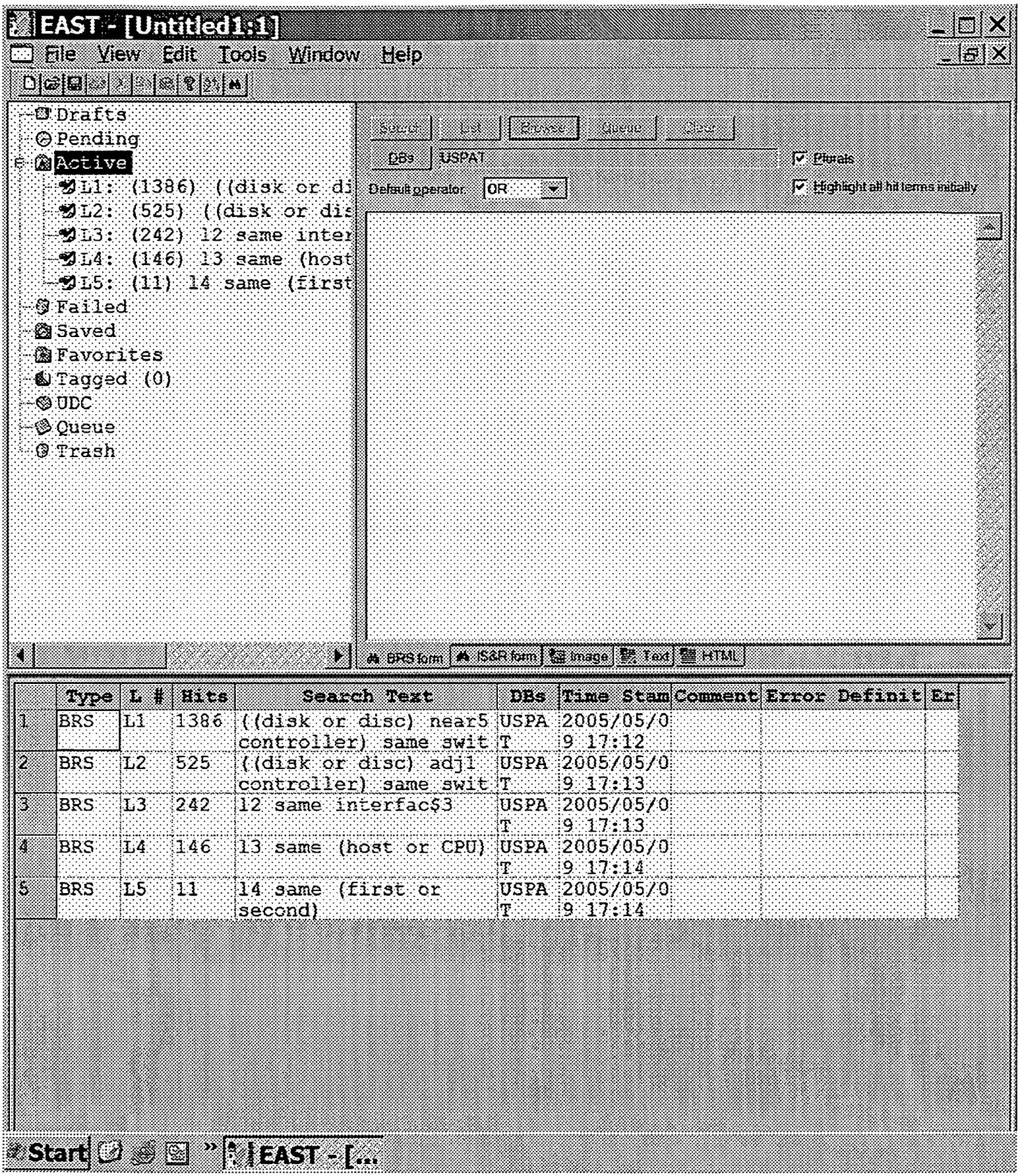
L4	L3 and switch	357	L4
L3	L2 same cache	679	L3
L2	L1 same memory	3899	L2
L1	((disk or disc) near05 controller) same (host or computer or CPU) same interfac$3	6955	L1

END OF SEARCH HISTORY



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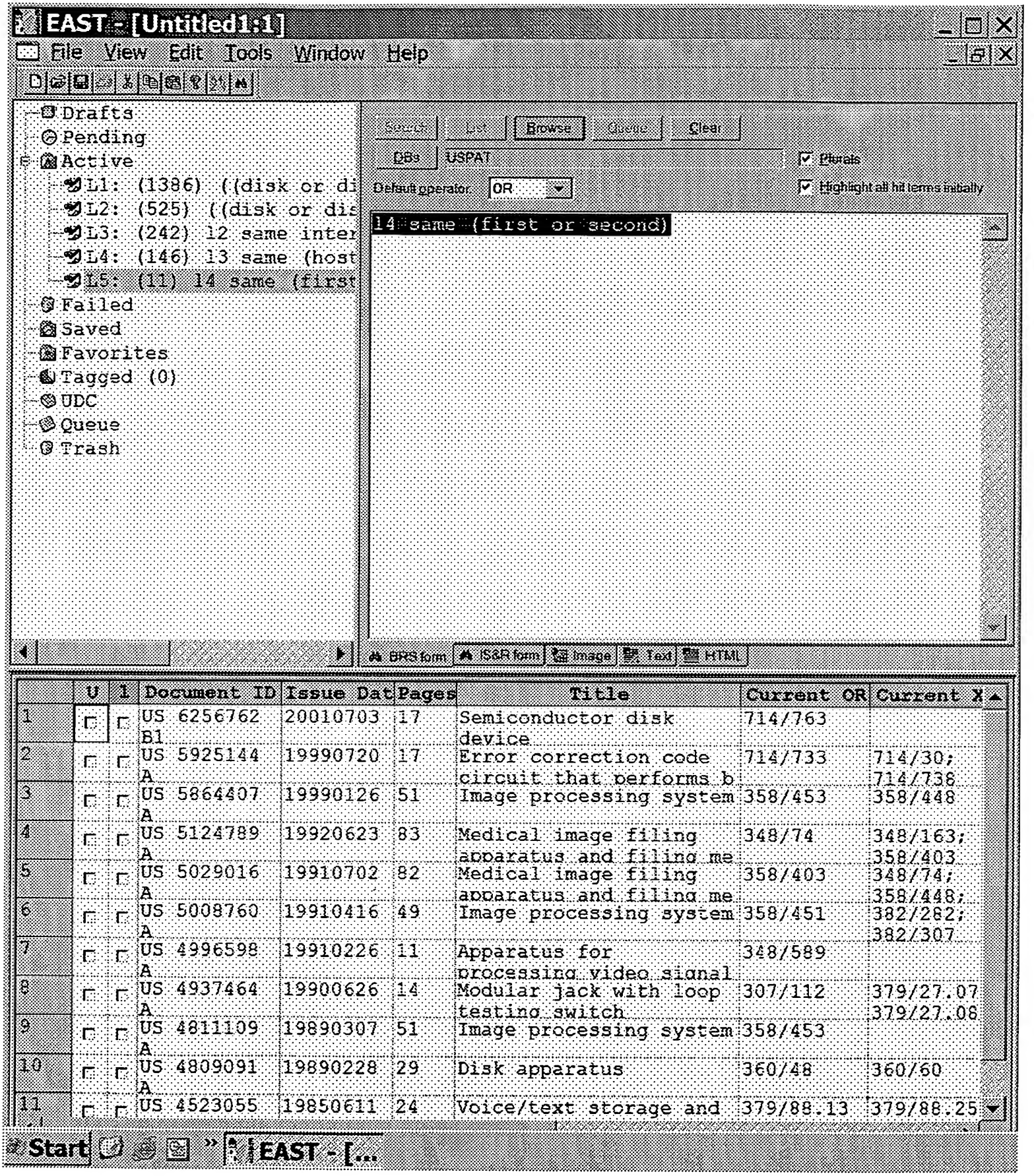
2	BRS	L2	525	((disk or disc) adj1 controller) same swit	USPAT	2005/05/09 17:13			
3	BRS	L3	242	12 same interfac$3	USPAT	2005/05/09 17:13			
4	BRS	L4	146	13 same (host or CPU)	USPAT	2005/05/09 17:14			
5	BRS	L5	11	14 same (first or second)	USPAT	2005/05/09 17:14			


EAST - [Untitled1:1]
File View Edit Tools Window Help
Drafts
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L1: (1386) ((disk or di
L2: (525) ((disk or dis
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L4: (146) 13 same (host
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Trash
Search
Browse
Queue
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Plurals
Default operator:
OR
Highlight all hit terms initially
14 same (first or second)
BRS form
IS&R form
Image
Text
HTML
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I
Document ID
Issue Dat
Pages
Title
Current OR
Current X
1 US 6256762 B1 20010703 17 Semiconductor disk device 714/763
2 US 5925144 A 19990720 17 Error correction code circuit that performs b 714/733 714/30; 714/738
3 US 5864407 A 19990126 51 Image processing system 358/453 358/448
4 US 5124789 A 19920623 83 Medical image filing apparatus and filing me 348/74 348/163; 358/403
5 US 5029016 A 19910702 82 Medical image filing apparatus and filing me 358/403 348/74; 358/448;
6 US 5008760 A 19910416 49 Image processing system 358/451 382/282; 382/307
7 US 4996598 A 19910226 11 Apparatus for processing video signal 348/589
8 US 4937464 A 19900626 14 Modular jack with loop testing switch 307/112 379/27.07 379/27.08
9 US 4811109 A 19890307 51 Image processing system 358/453
10 US 4809091 A 19890228 29 Disk apparatus 360/48 360/60
11 US 4523055 19850611 24 Voice/text storage and 379/88.13 379/88.25
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L9: Entry 6 of 6 File: USPT Mar 2, 2004

US-PAT-NO: 6701410
DOCUMENT-IDENTIFIER: US 6701410 B2

TITLE: Storage system including a switch

DATE-ISSUED: March 2, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Matsunami; Naoto	Sagamihara			JP
Oeda; Takashi	Sagamihara			JP
Yamamoto; Akira	Sagamihara			JP
Mimatsu; Yasuyuki	Fujisawa			JP
Sato; Masahiko	Odawara			JP

US-CL-CURRENT: 711/114; 711/130, 711/161, 711/162

ABSTRACT:

A disk storage system containing a storage device having a record medium for holding the data, a plurality of storage sub-systems having a controller for controlling the storage device, a first interface node coupled to a computer using the data stored in the plurality of storage sub-systems, a plurality of second interface nodes connected to the storage sub-systems, a switch connecting to a first interface node and a plurality of second interface nodes to perform frame transfer therebetween based on node address information added to the frame. The first interface node has a configuration table to store structural information for the memory storage system and in response to the frame sent from the computer, analyzes the applicable frame, converts information relating to the transfer destination of that frame based on structural information held in the configuration table, and transfers that frame to the switch.

29 Claims, 30 Drawing figures
Exemplary Claim Number: 27
Number of Drawing Sheets: 22

L9: Entry 6 of 6 File: USPT Mar 2, 2004

US-PAT-NO: 6701410
DOCUMENT-IDENTIFIER: US 6701410 B2

TITLE: Storage system including a switch

DATE-ISSUED: March 2, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Matsunami; Naoto	Sagamihara			JP
Oeda; Takashi	Sagamihara			JP
Yamamoto; Akira	Sagamihara			JP
Mimatsu; Yasuyuki	Fujisawa			JP
Sato; Masahiko	Odawara			JP

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Hitachi, Ltd.	Tokyo			JP	03

APPL-NO: 10/ 095578 [PALM]
DATE FILED: March 13, 2002

PARENT-CASE:
This is a continuation application of U.S. Ser. No. 09/468,327, filed on Dec. 21, 1999.

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	10-364079	December 22, 1998

INT-CL: [07] G06 F 12/00

US-CL-ISSUED: 711/114; 711/130, 711/161, 711/162
US-CL-CURRENT: 711/114; 711/130, 711/161, 711/162

FIELD-OF-SEARCH: 711/114, 711/130, 711/161, 711/162, 710/316, 710/317, 710/104, 710/8, 710/9, 710/10

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5140592	August 1992	Idleman et al.	714/5

☐	5237658	August 1993	Walker et al.	395/200
☐	5423046	June 1995	Nunnelley et al.	395/750
☐	5457703	October 1995	Kakuta et al.	714/766
☐	5574950	November 1996	Hathorn et al.	710/8
☐	5581735	December 1996	Kajitani et al.	711/169
☐	5606359	February 1997	Youden et al.	725/8B
☐	5729763	May 1998	Leshem	710/38
☐	5752256	May 1998	Fujii et al.	711/114
☐	5835694	November 1998	Hodges	711/114
☐	5974503	October 1999	Venkatesh et al.	711/114
☐	6098119	August 2000	Surugucchi et al.	710/10
☐	6105122	August 2000	Muller et al.	345/472
☐	6138176	October 2000	McDonald et al.	710/6
☐	6148349	November 2000	Chow et al.	709/214
☐	6173374	January 2001	Heil et al.	711/148
☐	6247077	June 2001	Muller et al.	710/74
☐	6253283	June 2001	Yamamoto	711/114
☐	6263374	July 2001	Olnowich et al.	709/253
☐	6289376	September 2001	Taylor et al.	709/219
☐	6493750	December 2002	Mathew et al.	709/220

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
980 041	February 2000	EP	
08/328760	December 1996	JP	
09/198308	July 1997	JP	
06-309186	November 1999	JP	

OTHER PUBLICATIONS

Chiang et al. "Implamentation of STARNET: A WDM Computer Communications Network", IEEE, pp. 824-839, Jun. 1996.*
"A Case for Redundant Arrays of Inexpensive Disks (RAID)", Proc. ACM SIGMOD, Jun. 1988, D. Patterson et al, pp. 109-116.
Serial SCSI Finally Arrives on the Market, NIKKEI ELCTRONICS, No. 639, 1995, p. 79.

ART-UNIT: 2186

PRIMARY-EXAMINER: Kim; Matthew

ASSISTANT-EXAMINER: Elmore; Stephen

ATTY-AGENT-FIRM: Mattingly, Stanger & Malur, P.C.

ABSTRACT:

A disk storage system containing a storage device having a record medium for holding the data,

a plurality of storage sub-systems having a controller for controlling the storage device, a first interface node coupled to a computer using the data stored in the plurality of storage sub-systems, a plurality of second interface nodes connected to the storage sub-systems, a switch connecting to a first interface node and a plurality of second interface nodes to perform frame transfer therebetween based on node address information added to the frame. The first interface node has a configuration table to store structural information for the memory storage system and in response to the frame sent from the computer, analyzes the applicable frame, converts information relating to the transfer destination of that frame based on structural information held in the configuration table, and transfers that frame to the switch.

29 Claims, 30 Drawing figures

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L9: Entry 5 of 6 File: USPT Mar 2, 2004

US-PAT-NO: 6701411
DOCUMENT-IDENTIFIER: US 6701411 B2

TITLE: Switch and storage system for sending an access request from a host to a storage subsystem

DATE-ISSUED: March 2, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Matsunami; Naoto	Sagamihara			JP
Oeda; Takashi	Sagamihara			JP
Yamamoto; Akira	Sagamihara			JP
Mimatsu; Yasuyuki	Fujisawa			JP
Sato; Masahiko	Odawara			JP

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Hitachi, Ltd.	Tokyo			JP	03

APPL-NO: 10/ 095581 [PALM]
DATE FILED: March 13, 2002

PARENT-CASE:
is a continuation application of U.S. Ser. No. 09/468,327, filed on Dec. 21, 1999, now U.S. Pat. No. 6,542,961.

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	10-364079	December 22, 1998

INT-CL: [07] G06 F 12/00

US-CL-ISSUED: 711/114; 711/130, 711/161, 711/162
US-CL-CURRENT: 711/114; 711/130, 711/161, 711/162

FIELD-OF-SEARCH: 711/114, 711/130, 711/161, 711/162, 710/316, 710/317, 710/104, 710/8, 710/9, 710/10

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5237658	August 1993	Walker et al.	395/200

☐	5423046	June 1995	Nunnelley et al.	395/750
☐	5457703	October 1995	Kakuta et al.	714/766
☐	5517662	May 1996	Coleman et al.	709/201
☐	5574950	November 1996	Hathorn et al.	395/861
☐	5752256	May 1998	Fujii et al.	711/114
☐	5835694	November 1998	Hodges	711/114
☐	5974503	October 1999	Venkatesh et al.	711/114
☐	6098119	August 2000	Surugucchi et al.	710/10
☐	6098129	August 2000	Fukuzawa et al.	710/65
☐	6098199	August 2000	Barkin	2/159
☐	6105122	August 2000	Muller et al.	345/472
☐	6138176	October 2000	McDonald et al.	710/6
☐	6148349	November 2000	Chow et al.	709/214
☐	6247077	June 2001	Muller et al.	710/74
☐	6253283	June 2001	Yamamoto	711/114
☐	6256740	July 2001	Muller et al.	713/201
☐	6263374	July 2001	Olnowich et al.	709/253
☐	6289376	September 2001	Taylor et al.	709/219
☐	6493750	December 2002	Mathew et al.	709/220

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
980 041	February 2000	EP	
06-309186	November 1994	JP	
08-328760	December 1996	JP	
09-198308	July 1997	JP	

OTHER PUBLICATIONS

Chiang et al, "Implementation of Starnet: A WDM Computer Communications Network," IEEE, pp. 824-839, Jun. 1996.
"A Case for Redundant Arrays of Inexpensive Disks (RAID)", Proc. ACM SIGMOD, Jun. 1988, D. Patterson et al, pp. 109-116.
Serial SCSI Finally Arrives on the Market, Nikkei Electronics, No. 639, 1995,p. 79.

ART-UNIT: 2186

PRIMARY-EXAMINER: Kim; Matthew

ASSISTANT-EXAMINER: Elmore; Stephen

ATTY-AGENT-FIRM: Mattingly, Stanger & Malur, P.C.

ABSTRACT:

A disk storage system containing a storage device having a record medium for holding the data, a plurality of storage sub-systems having a controller for controlling the storage device, a first interface node coupled to a computer using the data stored in the plurality of storage

sub-systems, a plurality of second interface nodes connected to the storage sub-systems, a switching connecting to a first interface node and a plurality of second interface nodes to perform frame transfer therebetween based on node address information added to the frame. The first interface node has a configuration table to store structural information for the memory storage system and in response to the frame sent from the computer, analyzes the applicable frame, converts information relating to the transfer destination of that frame based on structural information held in the configuration table, and transfers that frame to the switch.

26 Claims, 30 Drawing figures

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L9: Entry 5 of 6 File: USPT Mar 2, 2004

DOCUMENT-IDENTIFIER: US 6701411 B2
TITLE: Switch and storage system for sending an access request from a host to a storage subsystem

Abstract Text (1):
A disk storage system containing a storage device having a record medium for holding the data, a plurality of storage sub-systems having a controller for controlling the storage device, a first interface node coupled to a computer using the data stored in the plurality of storage sub-systems, a plurality of second interface nodes connected to the storage sub-systems, a switching connecting to a first interface node and a plurality of second interface nodes to perform frame transfer therebetween based on node address information added to the frame. The first interface node has a configuration table to store structural information for the memory storage system and in response to the frame sent from the computer, analyzes the applicable frame, converts information relating to the transfer destination of that frame based on structural information held in the configuration table, and transfers that frame to the switch.

Detailed Description Text (7):
The lower adapter 103 contains a lower MPU103 to execute control of the lower adapter 103, a disk I/F controller 1031 to control the disk 104 and interface which is the disk I/F, and a lower bus 1032 to perform communications and data transfer between the cache memory/shared memory 102 and host MPU1030 and the diskarray I/F controller 1031. The figure shows four diskarray I/F controllers 1031 for each lower adapter 103 however the number of diskarray I/F controllers is optional and can be changed according to the diskarray configuration and the number of disks that are connected.

L9: Entry 3 of 6 File: USPT Feb 1, 2005

US-PAT-NO: 6851029
DOCUMENT-IDENTIFIER: US 6851029 B2

TITLE: Disk storage system including a switch

DATE-ISSUED: February 1, 2005

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Matsunami; Naoto	Sagamihara			JP
Oeda; Takashi	Sagamihara			JP
Yamamoto; Akira	Sagamihara			JP
Mimatsu; Yasuyuki	Fujisawa			JP
Sato; Masahiko	Odawara			JP

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Hitachi, Ltd.	Tokyo			JP	03

APPL-NO: 10/ 405645 [PALM]
DATE FILED: April 3, 2003

PARENT-CASE:
This is a continuation application of U.S. Ser. No. 10/095,581, filed on Mar. 13, 2002, now U.S. Pat. No. 6,701,411 which is a continuation application of U.S. Ser. No. 09/468,327, filed on Dec. 21, 1999, now U.S. Pat. No. 6,542,961. This application is related to U.S. Ser. No. 10/095,578, filed Mar. 13, 2002 now U.S. Pat. No. 6,701,410.

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	10-364079	December 22, 1998

INT-CL: [07] G06 F 12/00

US-CL-ISSUED: 711/154; 711/114, 711/130, 711/161, 711/162, 710/316, 710/317, 710/104, 710/8, 710/9, 710/10, 709/220, 709/229, 709/232, 709/236
US-CL-CURRENT: 711/154; 709/220, 709/229, 709/232, 709/236, 710/10, 710/104, 710/316, 710/317, 710/8, 710/9, 711/114, 711/130, 711/161, 711/162

FIELD-OF-SEARCH: 711/154, 711/114, 711/130, 711/161, 711/162, 710/316, 710/317, 710/8, 710/104, 710/9, 710/10, 709/220, 709/229, 709/232, 709/236

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5140592	August 1992	Idleman et al.	714/5
☐	5237658	August 1993	Walker et al.	710/38
☐	5423046	June 1995	Nunnelley et al.	713/330
☐	5457703	October 1995	Kakuta et al.	714/766
☐	5517662	May 1996	Coleman et al.	709/201
☐	5574950	November 1996	Hathorn et al.	710/8
☐	5581735	December 1996	Kajitani et al.	711/169
☐	5606359	February 1997	Youden et al.	348/7
☐	5619690	April 1997	Matsumani et al.	707/200
☐	5729763	March 1998	Leshem	710/38
☐	5752256	May 1998	Fujii et al.	711/114
☐	5835694	November 1998	Hodges	714/6
☐	5974503	October 1999	Venkatesh et al.	711/114
☐	6098119	August 2000	Surugucchi et al.	710/10
☐	6098129	August 2000	Fukuzawa et al.	710/65
☐	6098199	August 2000	Barkin	2/159
☐	6105122	August 2000	Muller et al.	712/1
☐	6138176	October 2000	McDonald et al.	710/6
☐	6148349	November 2000	Chow et al.	710/33
☐	6173374	January 2001	Heil et al.	711/148
☐	6247077	June 2001	Muller et al.	710/74
☐	6253283	June 2001	Yamamoto	711/114
☐	6256740	July 2001	Muller et al.	713/201
☐	6263374	July 2001	Olnowich et al.	709/253
☐	6289376	September 2001	Taylor et al.	709/219
☐	6493750	December 2002	Mathew et al.	709/220
☐	6542961	April 2003	Matsunami et al.	711/114

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
980 041	February 2000	EP	
06-309186	November 1994	JP	
08/328760	December 1996	JP	
09-198308	July 1997	JP	

OTHER PUBLICATIONS

"A Case for Redundant Arrays of Inexpensive Disks (RAID)", Proc. ACM SIGMOD, Jun. 1988, D. Patterson et al, pp. 109-116.
Serial SCSI Finally Arrives on the Market, Nikkei Elctronics, No. 639, 1995,p. 79.
Chiang et al, "Implementation of STARNET: A WDM Computer Communications Network," IEEE, pp. 824-839, Jun. 1996.

ART-UNIT: 2186

PRIMARY-EXAMINER: Elmore; Stephen

ATTY-AGENT-FIRM: Mattingly, Stanger & Malur, P.C.

ABSTRACT:

A disk storage system containing a storage device having a record medium for holding the data, a plurality of storage sub-systems having a controller for controlling the storage device, a first interface node coupled to a computer using the data stored in the storage sub-systems, a plurality of second interface nodes connected to the storage sub-systems, a switch connecting to a first interface node and a plurality of second interface nodes to perform frame transfer therebetween based on node address information added to the frame. The first interface node has a configuration table to store structural information for the memory storage system and in response to the frame sent from the computer, analyzes the applicable frame, converts information relating to the transfer destination of that frame based on structural information held in the configuration table, and transfers that frame to the switch.

28 Claims, 30 Drawing figures

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L9: Entry 3 of 6 File: USPT Feb 1, 2005

DOCUMENT-IDENTIFIER: US 6851029 B2
TITLE: Disk storage system including a switch

Abstract Text (1):
A disk storage system containing a storage device having a record medium for holding the data, a plurality of storage sub-systems having a controller for controlling the storage device, a first interface node coupled to a computer using the data stored in the storage sub-systems, a plurality of second interface nodes connected to the storage sub-systems, a switch connecting to a first interface node and a plurality of second interface nodes to perform frame transfer therebetween based on node address information added to the frame. The first interface node has a configuration table to store structural information for the memory storage system and in response to the frame sent from the computer, analyzes the applicable frame, converts information relating to the transfer destination of that frame based on structural information held in the configuration table, and transfers that frame to the switch.

Detailed Description Text (7):
The lower adapter 103 contains a lower MPU103 to execute control of the lower adapter 103, a disk I/F controller 1031 to control the disk 104 and interface which is the disk I/F, and a lower bus 1032 to perform communications and data transfer between the cache memory/shared memory 102 and host MPU 1030 and the diskarray I/F controller 1031. The figure shows four diskarray I/F controllers 1031 for each lower adapter 103 however the number of diskarray I/F controllers is optional and can be changed according to the diskarray configuration and the number of disks that are connected.

L9: Entry 2 of 6 File: USPT Apr 19, 2005

DOCUMENT-IDENTIFIER: US 6883064 B2
TITLE: Disk array controller comprising a plurality of disk array controlling units

Abstract Text (1):
"Disk array system is presented wherein the plurality of disk array controlling units operate as the sole disk array controller so as to restrain the performance of the cache memory sections of the respective disk array controlling units from deteriorating owing to their physical packaging locations and to maximize the performance thereof in proportion to the number of the controlling units in use. Disk array controller is provided, which controller comprises a host switch interface section, the plurality of respective disk array controlling units provided with a channel interface section, a disc interface section and a cache memory section and a mutual connection network in connection with the channel interface sections, the disk interface sections and the cache memory sections of the respective disk array controlling units. Access performance to the cache memory sections that are dispersedly disposed between the respective disk array controlling units improves so as to enhance the performance of the disk array controller in proportion to the number of the disk array controlling units in use."

Brief Summary Text (7):
As a method for improving the I/O processing performance of the subsystem, a so-called disk array system is known wherein the subsystem comprises the plurality of magnetic disc units, into which disc units data are stored. This system generally comprises the plurality of magnetic disc units to record the I/O data from the higher order computer and a disk array controller to receive the I/O data from the computer and to transfer the same to the plurality of magnetic disc units. For the large-scale network connection and the large volume of communication, it may be arranged such that an ultra large-scale disk array controller is set up by connecting the plurality of disk array controllers of the conventional large-scale and high-end type. The connection of the plurality of disk array controllers allows cache memory to be dispersed into the respective controllers. For the performance's sake, it is advantageous that the cache memory stores the data of the magnetic disc units connected to the storage controller while the host computer getting access to the cache memory is connected to the storage controller having the same memory. However, the happening of packaging faults and the additional installation of the magnetic disc units and the storage controllers may cause the correspondence between the host interface section and the cache memory as well as between the cache memory and the magnetic disc controllers to alter from the above advantageous arrangements. Seen from the higher order apparatus and software systems as well as viewed from the conventional architectural continuation, it is advantageous that management is directed for the sole disk array controller rather than for an ultra large-scale disk array controller connecting the plurality of disk array controlling units. Restructuring caused by the connection of the host interface with the cache memory and the magnetic disc units or the additional installation thereof requires the packaging positions thereof to be optimized, which affects the performance of the disk array system more significantly than in the prior case where the system has been constructed by the sole disk array controller.

Brief Summary Text (8):
For instances, the prior disk array controller as shown in FIG. 2 is provided with the plurality of channel interface sections 11 to execute the data transfer between the host computer 50 and the disk array controllers 2, the plurality of the disc interface sections 12 to execute the data transfer between the magnetic disc units 5 and the disk array controllers 2 and the cache memory sections 14 to temporarily store the data of the magnetic disc units 5, wherein the cache memory sections 14 are accessible from all the channel interface sections 11 and the disc interface sections 12 within one disk array controller 2. In this disk array controller 2, a mutual connection network 21 intervenes between the channel interface section 11 and the cache memory section 14.

Brief Summary Text (13):
Another prior disk array controller as shown in FIG. 3 is provided with a host computer 50, disk array controllers 2, an external connection network 23 intervening between the host computer 50 and the disk array controllers, the plurality of channel interface sections 11 to execute the data transfer between the host computer 50 and the disk array controllers 2, the plurality of disc interface sections 12 to execute the data transfer between the magnetic disc units 5 and the disk array controllers 2 and the cache memory sections 14 to temporarily store the data of the magnetic disc units 5, wherein the host computer 50 is through the external connection network 23 accessible to all the disk array controllers 2 and it is arranged such that the cache memory sections 14 are accessible from all the channel interface sections 11 and the disc interface sections 12 within the sole disk array controller 2. In this prior art, a mutual connection network 21 intervenes between the interface sections 11 and 12 and the cache memory sections 14.

Brief Summary Text (18):
In order to solve the prior issues as mentioned above, the disk array controller according to the present invention comprises a host switch interface section, a plurality of respective disk array controlling units that are provided with a channel interface section having an interface with the host switch interface section, a disc interface section connected to a magnetic disc unit and a cache memory section to temporarily store the data read out of/written into the magnetic disc unit and a mutual connection network in connection with the plurality of the channel interface sections, the disc interface sections and the cache memory sections. It is further arranged such that the cache memory sections transfer the data with the channel interface sections of the whole disk array controlling units. It may be arranged such that a mutual connection network intervenes between the host switch interface section and the plurality of channel interface sections.

Detailed Description Text (5):
As shown in FIG. 1, a disk array controller 1 comprises the plurality of disk array controlling units 1-2 and a host switch interface section 30. The disk array controlling unit 1-2 is provided with an interface (a channel interface section) 11 with the host switch interface section 30, an interface section (a disc interface section) 12 with a magnetic disc unit 5 and a cache memory section 14, in which unit a mutual connection network 21 intervenes between the channel and disc interface sections 11 and 12 and the cache memory section 14. The cache memory sections 14 of the respective disk array controlling units 1-2 are interconnected through the mutual connection network 21. That is to say, it is arranged such that all of the channel interface sections 11 and the disc interface sections 12 are through the mutual connection network 21 accessible to all the cache memory sections 14. The mutual connection network 21 is arranged such that the data transfer performance thereof within a disk array controlling unit is superior to that by way of the plurality of disk array controlling units. That is because there is lighter burden on the mutual connection network when the data transfer is carried out through the channel interface section of the disk array controlling unit having the cache memory section to which the host computer gets access. Further, it is arranged between the host switch interface section 30 and the plurality of channel interface sections 11 of as many disk array controlling units 1-2 such that the same section 30 is accessible to all of the cache memory sections 14. The host switch interface section 30 is capable of selecting a specific channel interface section to be connected with the host computer among the plural interface sections 11 within as many disk array controlling units 1-2 in response to the request made by the host computer. A management table 31 is provided in the host switch interface section 30, which table stores host computer access and connection information.

Detailed Description Text (6):
With reference to FIG. 1, read-out operation from the cache memory section 14 within the disk array controlling unit 1-2 by the host computer 50 is pondered. The host switch interface section 30 refers to the management table 31 therein in response to the request (read-out/writing request) made by the host computer 50 so as to find an optimum route accessible to the cache memory 14 at target and to issue such request to the channel interface section 11 to which such optimum route is connected. The channel interface section 11 that receives such request gets access to the cache memory section 14 at target through the mutual connection network 21 on the basis of the address information so as to read out the data as requested. The host switch interface section 30 weighs the data volume so as to store the relevant information into the history information table within the management table 31 upon issuing the request from the host computer 50 to the channel interface section 11.

Detailed Description Text (7):
As shown in FIG. 4, the disk array controller 1 is provided with the plurality of disk array controlling units and the host switch interface section 30. FIG. 4 shows a disk array controlling unit (BOX0) 1-2-1, a disk array controlling unit (BOX1) 1-2-2 and a disk array controlling unit (BKBOX) 1-2-3. It is arranged in FIG. 4 such that the BKBOX is used as a back-up disk array controlling unit. The disk array controlling units (BOX0) 1-2-1, (BOX1) 1-2-2 and (BKBOX) 1-2-3 as shown in FIG. 4 respectively are provided with a channel interface section 11 interfacing with the host switch interface section 30, an interface section with the magnetic disc unit, which section is not shown in the drawing and a cache memory section 14 wherein a mutual connection network 21 that extends across the plurality of disk array controlling units intervenes between the channel interface sections 11 and the cache memory sections 14. The host switch interface section 30 is connected through a PATH050, a PATH151 and a PATHBK 52 with the plurality of channel interface sections of as many disk array controlling units. A management table 31 is provided in the host switch interface section 30, in which table a path selection table 32 and a history information table 33 are provided, from which information table a path selection signal 40 is output to the path selection table 32, on the basis of which signal a PATH NO. 41 is selected.

Detailed Description Text (8):
With reference to FIG. 4, the operation of the host switch interface section 30 is pondered when the host computer 50 gains access to the cache memory section 14 of the disk array controlling unit (BOX0) 1-2-1. Upon the arrival of a request from the host computer 50 to the host switch interface section 30, the path selection table 32 is referred to, and on the basis of the address as requested, the specific disk array controlling unit that packages the cache memory section 14 storing the data at the computer's request is discernable among the controlling units (BOX0) 1-2-1, (BOX1) 1-2-2 and (BKBOX) 1-2-3. It is supposed herein that the host computer makes a request to get access to the cache memory section 14 of the BOX01-2-1, so that this controlling unit is selected. The storage in the path selection table 32 in the form of the path numbers of the access route information to the respective cache memory sections 14 from the host switch interface section 30 allows the specific path candidates to be discerned on the basis of the address as requested and with reference to the table 32. It is supposed herein that the host computer makes a request to get access to the cache memory section 14 of the BOX01-2-1, so that PATH050, PATH151 and PATHBK 52 in correspondence for CANDIDATES 1, 2 and 3 are stored in the selection table. The number of the path candidates to be stored in the table 32 is arbitrary, three paths being exemplified in the present embodiment. The PATH050 is a path to connect the host switch interface section 30 with the BOX01-2-1 and the PATH151 being one to connect the same with the BOX11-2-2 while the PATHBK being one to connect the same with the BKBOX 1-2-3. Then, the path selection signal 40 that is output from the history information table 33 determines the specific path to be selected among PATH050, PATH151 and PATHBK 52. The path selection signal 40 is generated on the basis of the difference in weight between the candidates, whether it is over weighted mean and fault information and so forth wherein the history information table 33 weighs the data volume of the respective paths from the past requests by the host computer. The path selection signal 40 defines a PATH NO. 41, which determines an access route to the cache memory section. Where the PATH050 is selected, access is gained through the same from the host switch interface section 30 to the cache memory section 14 of the BOX01-2-1. Where the PATH151 is selected, access is gained from the host switch interface section 30 through the same PATH1 and via the channel interface section 11 of the BOX11-2-2 and by way of the mutual connection network 21 extending across the plurality of disk array controlling units to the cache memory section 14 of the BOX01-2-1 while the PATHBK 52 being selected, access is gained from the host switch interface section 30 through the same PATHBK and via the channel interface section 11 of BKBOX 1-2-3 and by way of the mutual connection network 21 extending across the plurality of disk array controlling units to the cache memory section 14 of the BOX01-2-1. Provided that the data volume of the respective paths in the table 33 is uniformly weighed, the PATH050 that is accessible in the shortest route is selected.

Detailed Description Text (10):
As shown in FIG. 5, the disk array controller 1 comprises the plurality of disk array controlling units 1-2 and the host switch interface section 30. A mutual connection network 22 intervenes between the host switch interface section 30 and the plurality of channel interface sections 11 of as many disk array controlling units 1-2. That is to say, access is gained from the host switch interface section 30 through the mutual connection network 22 to all of the cache memory sections 14. The mutual connection network 21 interconnecting the cache memory

sections 14 and the mutual connection network 22 to connect the host switch interface section 30 with the plurality of channel interface sections 11 of as many disk array controlling units 1-2 independently operate. The other arrangements of the modified example as mentioned above are the same as the embodiment as shown in FIG. 1.

Detailed Description Text (11):
With reference to FIG. 5, the read-out operation of the host computer 50 from the cache memory 14 of the disk array controlling unit 1-2 is pondered. The host switch interface section 30 upon the request of the host computer 50 refers to the management table 31 within the same section 30 and finds an optimum route accessible to the cache memory 14 at target so as to issue a request through the mutual connection network 22 to the channel interface section 11 to which such optimum route is connected. The operation of the modified example as mentioned above is the same as that of the embodiment as shown in FIG. 1, excepting that the request from the host switch interface section 30 is issued through the mutual connection network 22.

Detailed Description Text (12):
With reference to FIG. 6, the arrangement of the modified example as mentioned above is the same as that of the embodiment as shown in FIG. 4, excepting that the mutual connection network 22 intervenes between the host switch interface section 30 and the disk array controlling units as to the arrangement and control of the path selection table and the history information table within the management table 31. The PATH050 is a path to connect the mutual connection network 22 with the BOX01-2-1 and the PATH151 is a path to connect the same network with the BOX 1-2-2 while the PATHBK 52 is a path to connect the same network with the BKBOX 1-2-3. In the path selection table 32, the access route information of the respective cache memory sections 14 from the mutual connection network 22 is stored as the path numbers. Accordingly, with reference to the path selection table 32, the address as requested results in the relevant path candidates being discernable. It is supposed herein that the host computer makes a request to get access to the cache memory section 14 of the BOX01-2-1, so that a PATH 50, a PATH151 and a PATHBK 52 in correspondence for CANDIDATES 1, 2 and 3 are stored therein. The number of the path candidates to be stored in the table 32 is arbitrary, three paths being exemplified in the present embodiment. Then, the path selection signal 40 that is output from the history information table 33 determines the specific path to be selected among the PATH050, the PATH151 and the PATHBK 52. The path selection signal 40 defines a PATH No. 41, which leads to the determination of the access route to the cache memory at target. Where the PATH050 is selected, access is gained from the host switch interface section 30 through the mutual connection network 22 and via the same PATH0 to the cache memory section 14 of the BOX01-2-1. Where the PATH151 is selected, access is gained from the host switch interface section 30 through the mutual connection network 22 and via the same PATH1 and by way of the channel interface section 11 of the BOX11-2-2 and the mutual connection network 21 extending across the plurality of disk array controlling units to the cache memory section 14 of the BOX01-2-1 while the PATHBK 52 being selected, access is gained from the host switch interface section 30 through the mutual connection network 22 and via the same PATHBK and by way of the channel interface section 11 of the BKBOX 1-2-3 and the mutual connection network 22 extending across the plurality of disk array controlling units to the cache memory 14 of the BOX01-2-1.

Detailed Description Text (15):
The present embodiment is characterized in that the disk array controlling unit (BKBOX) 1-2-3 is used also at the normal operation of the disk array controller, in which unit a high-speed cache memory section 15 is provided. The other arrangements thereof are the same as the first embodiment as shown in FIG. 4. With reference to FIG. 5, the operation of the host switch interface section 30 for the data transfer with high-speed access is pondered. Upon the arrival of a request from the host computer 50 to the host switch interface section 30, the path selection table 32 within the management table 31 is referred to. Based on the address as requested, it is recognizable that the data at the computer's request is packaged in the high-speed cache memory 15. The path selection signal 40 that is output from the history information table 33 causes the PATHBK 52 to be selected wherein access is gained from the host switch interface section 30 through the same PATHBK to the high-speed cache memory section 15 of the BKBOX 1-2-3. In this way, the provision of such high-speed cache memory in the specific disk array controlling unit and the effective use of the management table 31 of the host switch interface section 30 well satisfy a highly demanding request from the host computer. It is of course that the capacity of the cache memory may be altered or the paths may be transmitted with higher speed. Further, in the same way as the modified example as shown in FIG. 6, the mutual connection network may intervene between the host switch interface section 30 and the disk array controlling units. In this case, as mentioned above, the paths as stored in the path

selection table 32 and as selected based on the history information table 33 are shared between the mutual connection network 22 and the disk array controlling units.

Detailed Description Text (18):
The present embodiment is the same as the first one as shown in FIG. 4, excepting for the provision of a resource management section 16 in the respective disk array controlling units, the provision of an operating ratio management table 34 in the management table 31 of the host switch interface section 30 and the connection of an operating ratio report signal 53 to the operating ratio management table 34 thereof from the resource management section 16 of the respective disk array controlling units. The management section 16 of the respective disk array controlling units manages the operating ratio of such resources as the cache memory 14 thereof, the channel interface sections 11 thereof and the disc interface sections thereof, which are not shown in the drawings, the mutual connection network 21 extending across the respective disk array controlling units and the internal paths as well as buffers thereof. The operating ratio information is reported to the management table 34 through the report signal 53, which table weighs the respective paths on the basis of the operating ratio report signal 53 transmitted from the respective disk array controlling units. The other 40 operations of the present embodiment are the same as those of the first one. Alternatively, in the same way as the modified example of the first embodiment as shown in FIG. 6, the mutual connection network may intervene between the host switch interface section 30 and the disk array controlling units. In this case, as mentioned above, the paths as stored in the path selection table 32 and as selected based on the history information table 33 are shared between the mutual connection network 22 and the disk array controlling units.

Detailed Description Text (20):
According to the present invention, where the sole disk array controller operates as the plurality of disk array controlling units, the optimum connection route is secured between the host computer and the cache memory of the respective disk array controlling units, even if the cache memory is dispersedly packaged in the respective units, which allows such resources as mentioned above to be utilized in the most suitable way. Further, without the host computer being aware of the physical packaging locations of the cache memory sections and irrespective of the packaging locations thereof, the constant cache memory access is provided as the sole disk array controller. Further, the mutual connection network extending across the cache memory sections of the respective disk array controlling units operates independently from that to connect the host switch interface section with the respective channel interface sections, which allows the request from the host switch interface section to be distributed intact into the respective disk array controlling units.

CLAIMS:

1. A disk array controller comprising: a host switch interface section that is connected to a host computer; a plurality of respective disk array controlling units that are provided with a channel interface section interfacing with said host switch interface section, a disc interface section that is connected to a magnetic disc unit and a cache memory section that temporarily stores data as read out of or written into said magnetic disc unit; and a mutual connection network in connection with the channel interface sections, the disc interface sections and the cache memory sections of said disk array controlling units, wherein said cache memory sections perform a transfer of the data with the channel interface sections of said respective disk array controlling units, wherein in case of transferring a copy of data stored in said magnetic disk unit which is associated with first disk, array controlling unit included in said plurality of disk array controlling units, from said first disk array controlling unit to a second disk array controlling unit included in said plurality of disk array controlling units, said first disk array controlling unit performs a transfer of said copy of data via said mutual connection network, not via said host switch interface section, and wherein said host switch interface section selects a relay destination for data which is sent from said host computer to said cache memory section in said first disk array controlling unit, from the channel interface section in said first disk array controlling unit, the channel interface section in said second disk array controlling unit, or the channel interface section in another disk array controlling unit included in said plurality of disk array controlling units other than said first and second disk array controlling units, in accordance with load conditions of a path to said cache memory section in said first disk array controlling unit through said first disk array controlling unit, through said second disk array controlling unit, and through said another disk array controlling unit included in said plurality of disk array controlling units.

7. A disk array controller comprising: a host switch interface section that is connected to a host computer; a plurality of respective disk array controlling units that are provided with a channel interface section interfacing with said host switch interface section, a disc interface section that is connected to a magnetic disc unit and a cache memory section that temporarily stores data as read out of or written into said magnetic disc unit; a first mutual connection network in connection with the channel interface sections, the disc interface sections and the cache memory sections of said respective disk array controlling units; and a second mutual connection network in connection with said host interface section and the channel interface sections of said respective disk array controlling units, wherein said cache memory sections perform a transfer of the data with the channel interface sections of said respective disk array controlling units, wherein in case of transferring a copy of data stored in said magnetic disk unit which is associated with ea4da first disk array controlling unit included in said plurality of disk array controlling units, from said first disk array controlling unit to a second disk array controlling unit included in said plurality of disk array controlling units, said first disk array controlling unit performs a transfer of said copy of data via said first mutual connection network, not via said host switch interface section, and wherein said host switch interface section selects a relay destination for data which is sent from said host computer to said cache memory section in said first disk array controlling unit, from the channel interface section in said first disk array controlling unit, the channel interface section in said second disk array controlling unit, or the channel interface section in another disk array controlling unit included in said plurality of disk array controlling units other than said first and second disk controlling units, in accordance with load conditions of a path to said cache memory section in said first disk array controlling unit through said first disk array controlling unit, through said second disk array controlling unit, and through said another disk array controlling unit included in said plurality of disk array controlling units.

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[54] **DISK APPARATUS**

[75] Inventors: Shoichi Miyazawa; Satoshi Kawamura, both of Yokohama; Shoichiro Tetsuma; Odawara; Akira Ishihashi, Tokyo; Kazutoshi Kato, Narashino; Junichi Ideta, Tokyo, all of Japan

[73] Assignees: Hitachi, Ltd.; Tokico Ltd., both of Tokyo, Japan

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Primary Examiner—Vincent P. Canney
Attorney, Agent, or Firm—Antonelli, Terry & Wands

[57] **ABSTRACT**

A disk drive system includes a magnetic disk apparatus which accurately positions read/write heads for reading data from and writing data on tracks on the data surface of a rotary disk on a predetermined track on the disk on the basis of servo data written in the servo area formed on the data surface, and a disk controller which controls the mode of operation of the disk apparatus. Index signals respectively indicating the start and end of the servo area are generated on the basis of the result of detection of the angular phase of the disk. The mode of operation of the magnetic disk apparatus is determined on the basis of a write control signal provided by the disk controller. The index signals respectively indicating the start and end of the servo area are sent to the disk controller when the mode of operation is track format write mode, while the index signal indicating the end of the servo area is sent to the disk controller when the mode of operation is other than the track format write mode.

17 Claims, 20 Drawing Sheets